WHAT IS CLAIMED IS:

1. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a dielectric body and a first interconnection scheme, wherein the first interconnection scheme interlaces inside the dielectric body of the first built-up layer and is electrically connected to the electric devices;

a passivation layer disposed on the first built-up layer and provided with at least one opening exposing the first interconnection scheme; and

a second built-up layer arranged over the passivation layer, the second built-up layer provided with a second interconnection scheme, the second interconnection scheme electrically connected to the first interconnection layer with passing through the opening of the passivation layer, the trace thickness of the second interconnection scheme larger than that of the first interconnection scheme, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

2. The chip structure according to claim 1, wherein the trace thickness of the second interconnection scheme ranges from 1 micron to 50 microns.

3. The chip structure according to claim 1, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

4. The chip structure according to claim 1, wherein the second built-up layer further includes a dielectric body and the second interconnection scheme interlaces inside the dielectric body of the second built-up layer.

5. The chip structure according to claim 4, wherein the dielectric body of the second built-up layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

6. The chip structure according to claim 1, wherein the second interconnection scheme includes at least one metal layer and at least one via metal filler, the metal layer is electrically connected with the via metal filler, the via metal filler is electrically connected to the first interconnection scheme with passing through the opening of the passivation layer, and the cross-sectional area of the via metal filler is larger than that of the opening of the passivation layer.

7. The chip structure according to claim 1, wherein the largest width of the opening of the passivation layer ranges from 0.5 microns to 200 microns.

8. The chip structure according to claim 1, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

9. The chip structure according to claim 1, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first

interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

10. The chip structure according to claim 9, wherein the transition device is a driver, a receiver or an I/O circuit.

11. The chip structure according to claim 1, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the openings of the passivation layer expose the first conductive pad and the second conductive pad, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

12. The chip structure according to claim 11, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

13. The chip structure according to claim 12, wherein the linking trace is shorter than 5,000 microns.

14. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a dielectric body and a first interconnection scheme, wherein

the first interconnection scheme interlaces inside the dielectric body of the first built-up layer and is electrically connected to the electric devices;

a passivation layer disposed on the first built-up layer and provided with at least one opening exposing the first interconnection scheme; and

a second built-up layer arranged over the passivation layer, the second built-up layer provided with a second interconnection scheme, the second interconnection scheme electrically connected to the first interconnection layer with passing through the opening of the passivation layer, the trace width of the second interconnection scheme larger than that of the first interconnection scheme, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

15. The chip structure according to claim 14, wherein the trace width of the second interconnection scheme ranges from 1 micron to 1 centimeter.

16. The chip structure according to claim 14, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

17. The chip structure according to claim 14, wherein the second built-up layer further includes a dielectric body and the second interconnection scheme interlaces inside the dielectric body of the second built-up layer.

18. The chip structure according to claim 17, wherein the dielectric body of the second built-up layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

19. The chip structure according to claim 14, wherein the second interconnection scheme includes at least one metal layer and at least one via metal filler, the metal layer is electrically connected with the via metal filler, the via metal filler is electrically connected to the first interconnection scheme with passing through the opening of the passivation layer, and the cross-sectional area of the via metal filler is larger than that of the opening of the passivation layer.

20. The chip structure according to claim 14, wherein the largest width of the opening of the passivation layer ranges from 0.5 microns to 200 microns.

21. The chip structure according to claim 14, wherein at least one of the electric devices is an electrostatic discharge circuit and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

22. The chip structure according to claim 14, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

23. The chip structure according to claim 22, wherein the transition device is

a driver, a receiver or an I/O circuit.

24. The chip structure according to claim 14, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the openings of the passivation layer expose the first conductive pad and the second conductive pad, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

25. The chip structure according to claim 24, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

26. The chip structure according to claim 25, wherein the linking trace is shorter than 5,000 microns.

27. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a dielectric body and a first interconnection scheme, wherein the first interconnection scheme interlaces inside the dielectric body of the first built-up layer and is electrically connected to the electric devices;

a passivation layer disposed on the first built-up layer and provided with at least one opening exposing the first interconnection scheme; and

a second built-up layer arranged over the passivation layer, the second built-up layer provided with a second interconnection scheme, the second interconnection

scheme electrically connected to the first interconnection layer with passing through the opening of the passivation layer, the cross-sectional area of the traces of the second interconnection scheme larger than that of the traces of the first interconnection scheme, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

28. The chip structure according to claim 27, wherein the cross area of the traces of the second interconnection scheme ranges from 1 square micron to 0.5 square millimeters.

29. The chip structure according to claim 27, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

30. The chip structure according to claim 27, wherein the second built-up layer further includes a dielectric body and the second interconnection scheme interlaces inside the dielectric body of the second built-up layer.

31. The chip structure according to claim 30, wherein the dielectric body of the second built-up layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

32. The chip structure according to claim 27, wherein the second

interconnection scheme includes at least one metal layer and at least one via metal filler, the metal layer is electrically connected with the via metal filler, the via metal filler is electrically connected to the first interconnection scheme with passing through the opening of the passivation layer, and the cross-sectional area of the via metal filler is larger than that of the opening of the passivation layer.

33. The chip structure according to claim 27, wherein the largest width of the opening of the passivation layer ranges from 0.5 microns to 200 microns.

34. The chip structure according to claim 27, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

35. The chip structure according to claim 27, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

36. The chip structure according to claim 35, wherein the transition device is a driver, a receiver or an I/O circuit.

37. The chip structure according to claim 27, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the openings of the passivation layer expose the first conductive pad

and the second conductive pad, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

38. The chip structure according to claim 37, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

39. The chip structure according to claim 38, wherein the linking trace is shorter than 5,000 microns.

40. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a first dielectric body and a first interconnection scheme, the first interconnection scheme interlacing inside the first dielectric body, the first interconnection scheme electrically connected to the electric devices, the first interconnection scheme including a plurality of first metal layers and a plurality of plugs, and the neighbored first metal layers electrically connected through the plugs;

a passivation layer disposed on the first built-up layer and provided with at least one opening exposing the first interconnection scheme; and

a second built-up layer arranged over the passivation layer, the second built-up layer provided with a second dielectric body and a second interconnection scheme, the second interconnection scheme interlacing inside the second dielectric body, the second interconnection scheme electrically connected to the first interconnection layer

with passing through the opening of the passivation layer, the second interconnection scheme including at least one second metal layer and at least one via metal filler, the second metal layer electrically connected with the via metal filler, the cross-sectional area of the via metal filler larger than that of the plugs, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

41. The chip structure according to claim 40, wherein the cross area of the via metal filler ranges from 1 square micron to 10,000 square microns.

42. The chip structure according to claim 40, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

43. The chip structure according to claim 40, wherein the second dielectric body is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

44. The chip structure according to claim 40, wherein the cross-sectional area of the via metal filler is larger than that of the opening of the passivation layer.

45. The chip structure according to claim 40, wherein the largest width of the opening of the passivation layer ranges from 0.5 microns to 200 microns.

46. The chip structure according to claim 40, wherein at least one of the

electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

47. The chip structure according to claim 40, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

48. The chip structure according to claim 47, wherein the transition device is a driver, a receiver or an I/O circuit.

49. The chip structure according to claim 40, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the openings of the passivation layer expose the first conductive pad and the second conductive pad, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

50. The chip structure according to claim 49, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

51. The chip structure according to claim 50, wherein the linking trace is shorter than 5,000 microns.

52. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a first dielectric body and a first interconnection scheme, the first interconnection scheme interlacing inside the first dielectric body, the first interconnection scheme electrically connected to the electric devices, and the first dielectric body composed of at least one first dielectric layer;

a passivation layer disposed on the first built-up layer and provided with at least one opening exposing the first interconnection scheme; and

a second built-up layer arranged over the passivation layer, the second built-up layer provided with a second dielectric body and a second interconnection scheme, the second interconnection scheme interlacing inside the second dielectric body, the second interconnection scheme electrically connected to the first interconnection layer with passing through the opening of the passivation layer, the second dielectric body composed of at least one second dielectric layer, the second dielectric layer thicker than the first dielectric layer, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

53. The chip structure according to claim 52, wherein the thickness of the

second dielectric layer ranges from 1 micron to 100 microns.

54. The chip structure according to claim 52, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

55. The chip structure according to claim 52, wherein the second dielectric body is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

56. The chip structure according to claim 52, wherein the second interconnection scheme includes at least one metal layer and at least one via metal filler, the metal layer is electrically connected with the via metal filler, the via metal filler is electrically connected to the first interconnection scheme with passing through the opening of the passivation layer, and the cross-sectional area of the via metal filler is larger than that of the opening of the passivation layer.

57. The chip structure according to claim 52, wherein the largest width of the opening of the passivation layer ranges from 0.5 microns to 200 microns.

58. The chip structure according to claim 52, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

59. The chip structure according to claim 52, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, then passes through the passivation layer, and finally is

transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

60. The chip structure according to claim 59, wherein the transition device is a driver, a receiver or an I/O circuit.

61. The chip structure according to claim 52, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the openings of the passivation layer expose the first conductive pad and the second conductive pad, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

62. The chip structure according to claim 61, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

63. The chip structure according to claim 62, wherein the linking trace is shorter than 5,000 microns.

64. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a dielectric body and a first interconnection scheme, wherein the first interconnection scheme interlaces inside the dielectric body of the first built-up

layer and is electrically connected to the electric devices; and

a second built-up layer arranged over the first built-up layer, the second built-up layer provided with a second interconnection scheme, the second interconnection scheme electrically connected with the first interconnection layer, the trace thickness of the second interconnection scheme larger than 1 micron, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

65. The chip structure according to claim 64, wherein the trace thickness of the second interconnection scheme ranges from 1 micron to 50 microns.

66. The chip structure according to claim 64, wherein the second built-up layer further includes a dielectric body and the second interconnection scheme interlaces inside the dielectric body of the second built-up layer.

67. The chip structure according to claim 66, wherein the dielectric body of the second built-up layer is made of an organic compound.

68. The chip structure according to claim 66, wherein the dielectric body of the second built-up layer is made of a macromolecule polymer.

69. The chip structure according to claim 66, wherein the dielectric body of the second built-up layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

70. The chip structure according to claim 64, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge

circuit is electrically connected with the first interconnection scheme.

71. The chip structure according to claim 64, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

72. The chip structure according to claim 71, wherein the transition device is a driver, a receiver or an I/O circuit.

73. The chip structure according to claim 64, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the first conductive pad and the second conductive pad are exposed outside the first built-up layer, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

74. The chip structure according to claim 73, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

75. The chip structure according to claim 74, wherein the linking trace is shorter than 5,000 microns.

76. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a

surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a dielectric body and a first interconnection scheme, wherein the first interconnection scheme interlaces inside the dielectric body of the first built-up layer and is electrically connected to the electric devices; and

a second built-up layer arranged over the first built-up layer, the second built-up layer provided with a second interconnection scheme, the second interconnection scheme electrically connected with the first interconnection layer, the trace width of the second interconnection scheme larger than 1 micron, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

77. The chip structure according to claim 76, wherein the trace width of the second interconnection scheme ranges from 1 micron to 1 centimeter.

78. The chip structure according to claim 76, wherein the second built-up layer further includes a dielectric body and the second interconnection scheme interlaces inside the dielectric body of the second built-up layer.

79. The chip structure according to claim 78, wherein the dielectric body of the second built-up layer is made of an organic compound.

80. The chip structure according to claim 78, wherein the dielectric body of the second built-up layer is made of a macromolecule polymer.

81. The chip structure according to claim 78, wherein the dielectric body of

the second built-up layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

82. The chip structure according to claim 76, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

83. The chip structure according to claim 76, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

84. The chip structure according to claim 83, wherein the transition device is a driver, a receiver or an I/O circuit.

85. The chip structure according to claim 76, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the first conductive pad and the second conductive pad are exposed outside the first built-up layer, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

86. The chip structure according to claim 85, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

87. The chip structure according to claim 86, wherein the linking trace is shorter than 5,000 microns.

88. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a dielectric body and a first interconnection scheme, wherein the first interconnection scheme interlaces inside the dielectric body of the first built-up layer and is electrically connected to the electric devices; and

a second built-up layer arranged over the first built-up layer, the second built-up layer provided with a second interconnection scheme, the second interconnection scheme electrically connected with the first interconnection layer, the cross-sectional area of the traces of the second interconnection scheme larger than 1 square micron, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

89. The chip structure according to claim 88, wherein the trace width of the second interconnection scheme ranges from 1 square micron to 0.5 square millimeters.

90. The chip structure according to claim 88, wherein the second built-up layer further includes a dielectric body and the second interconnection scheme interlaces inside the dielectric body of the second built-up layer.

91. The chip structure according to claim 90, wherein the dielectric body of the second built-up layer is made of an organic compound.

92. The chip structure according to claim 90, wherein the dielectric body of the second built-up layer is made of a macromolecule polymer.

93. The chip structure according to claim 90, wherein the dielectric body of the second built-up layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

94. The chip structure according to claim 88, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

95. The chip structure according to claim 88, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

96. The chip structure according to claim 95, wherein the transition device is a driver, a receiver or an I/O circuit.

97. The chip structure according to claim 88, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the first conductive pad and the second conductive pad are exposed outside the first built-up layer, the second conductive pad is electrically connected with

the second interconnection scheme, and the first conductive pad is exposed to the outside.

98. The chip structure according to claim 97, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

99. The chip structure according to claim 98, wherein the linking trace is shorter than 5,000 microns.

100. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a first dielectric body and a first interconnection scheme, the first interconnection scheme interlacing inside the first dielectric body, the first interconnection scheme electrically connected to the electric devices, the first interconnection scheme including a plurality of first metal layers and a plurality of plugs, the plugs located between the neighbored first metal layers and the neighbored first metal layers electrically connected through the plugs; and

a second built-up layer arranged over the first built-up layer, the second built-up layer provided with a second dielectric body and a second interconnection scheme, the second interconnection scheme interlacing inside the second dielectric body, the second interconnection scheme electrically connected with the first interconnection layer, the second interconnection scheme including at least one second metal layer and at least one via metal filler, the second metal layer electrically connected with the via

metal filler, the cross-sectional area of the via metal filler larger than 1 square meter, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

101. The chip structure according to claim 100, wherein the cross-sectional area of the via metal filler ranges from 1 square micron to 10,000 square microns.

102. The chip structure according to claim 100, wherein the second dielectric body is made of an organic compound.

103. The chip structure according to claim 100, wherein the second dielectric body is made of a macromolecule polymer.

104. The chip structure according to claim 100, wherein the second dielectric body is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

105. The chip structure according to claim 100, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

106. The chip structure according to claim 100, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to

the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

107. The chip structure according to claim 106, wherein the transition device is a driver, a receiver or an I/O circuit.

108. The chip structure according to claim 100, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the first conductive pad and the second conductive pad are exposed outside the first built-up layer, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

109. The chip structure according to claim 108, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

110. The chip structure according to claim 109, wherein the linking trace is shorter than 5,000 microns.

111. A chip structure, comprising:

a substrate having a plurality of electric devices that are disposed on a surface of the substrate;

a first built-up layer located on the surface of the substrate, and the first built-up layer including a first dielectric body and a first interconnection scheme, the first interconnection scheme interlacing inside the first dielectric body, and the first interconnection scheme electrically connected to the electric devices; and

a second built-up layer arranged over the first built-up layer, the second

built-up layer provided with a second dielectric body and a second interconnection scheme, the second interconnection scheme interlacing inside the second dielectric body, the second interconnection scheme electrically connected with the first interconnection layer, the second dielectric body composed of at least one second dielectric layer, the thickness of the second dielectric layer larger than 1 micron, wherein a signal is transmitted from one of the electric devices to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

112. The chip structure according to claim 111, wherein the thickness of the second dielectric layer ranges from 1 micron to 100 microns.

113. The chip structure according to claim 111, wherein the second dielectric body is made of an organic compound.

114. The chip structure according to claim 111, wherein the second dielectric body is made of a macromolecule polymer.

115. The chip structure according to claim 111, wherein the second dielectric body is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

116. The chip structure according to claim 111, wherein at least one of the electric devices is an electrostatic discharge circuit, and the electrostatic discharge circuit is electrically connected with the first interconnection scheme.

117. The chip structure according to claim 111, wherein at least one of the electric devices is a transition device, the transition device is electrically connected with

the first interconnection scheme, a signal is transmitted from the transition device to the first interconnection scheme, and then is transmitted to the second interconnection scheme, and further, the signal is transmitted from the second interconnection scheme to the first interconnection scheme, and finally is transmitted to the other one or more of the electric devices.

118. The chip structure according to claim 117, wherein the transition device is a driver, a receiver or an I/O circuit.

119. The chip structure according to claim 111, wherein the first interconnection scheme includes at least one first conductive pad and at least one second conductive pad, the first conductive pad and the second conductive pad are exposed outside the first built-up layer, the second conductive pad is electrically connected with the second interconnection scheme, and the first conductive pad is exposed to the outside.

120. The chip structure according to claim 119, wherein the first interconnection scheme further includes at least one linking trace, through which the first conductive pad is electrically connected with the second conductive pad.

121. The chip structure according to claim 120, wherein the linking trace is shorter than 5,000 microns.

122. The process for fabricating a chip structure, comprising:

Step 1: providing a wafer with a plurality of electric devices, an interconnection scheme and a passivation layer, both the electric devices and the interconnection scheme arranged inside the wafer, the interconnection scheme electrically connected with the electric devices, the passivation layer disposed on a

surface layer of the wafer, the passivation layer having at least one opening exposing the interconnection scheme;

Step 2: forming a conductive layer over the passivation layer of the wafer and the conductive layer electrically connected with the interconnection scheme;

Step 3: forming a photoresist onto the conductive layer, and the photoresist having at least one opening exposing the conductive layer;

Step 4: filling at least one conductive metal over the conductive layer;

Step 5: removing the photoresist; and

Step 6: removing the conductive layer not covered with the conductive metal, wherein a signal is transmitted from one of the electric devices to the interconnection scheme, then passes through the passivation layer, and finally is transmitted to the conductive metal, and further, the signal is transmitted from the conductive metal to the interconnection scheme with passing through the passivation layer, and finally is transmitted to the other one or more of the electric devices.

123. The process according to claim 122, wherein a dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after step 6 is performed.

124. The process according to claim 123, wherein at least one node opening is formed through the dielectric sub-layer to expose the conductive metal formed at a lower portion after the dielectric sub-layer is formed over the passivation layer.

125. The process according to claim 123, wherein the dielectric sub-layer is made of an organic compound.

126. The process according to claim 123, wherein the dielectric sub-layer is

made of a macromolecule polymer.

127. The process according to claim 123, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

128. The process according to claim 122, wherein the process further comprises:

Step 7: forming a dielectric sub-layer over the passivation layer, the dielectric sub-layer covering the formed conductive metal, and the dielectric sub-layer having at least one opening exposing the conductive metal formed at a lower portion;

Step 8: forming at least other one conductive layer on the dielectric sub-layer and into the opening of the dielectric sub-layer, and the other conductive layer electrically connected with the metal layer exposed by the opening of the dielectric sub-layer;

Step 9: forming a photoresist onto the other conductive layer, and the photoresist having at least one opening exposing the other conductive layer;

Step 10: filling other at least one conductive metal into the opening of the photoresist, and the other conductive metal disposed over the other conductive layer;

Step 11: removing the photoresist; and

Step 12: removing the other conductive layer not covered with the other conductive metal.

129. The process according to claim 128, wherein the dielectric sub-layer is made of an organic compound.

130. The process according to claim 128, wherein the dielectric sub-layer is

made of a macromolecule polymer.

131. The process according to claim 128, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

132. The process according to claim 128, wherein the thickness of the dielectric sub-layer ranges from 1 micron to 100 microns.

133. The process according to claim 128, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the step 12 is performed.

134. The process according to claim 133, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

135. The process according to claim 133, wherein the other dielectric sub-layer is made of an organic compound.

136. The process according to claim 133, wherein the other dielectric sub-layer is made of a macromolecule polymer.

137. The process according to claim 133, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

138. The process according to claim 128, wherein the sequential steps 7-12 are repeated at least one time.

139. The process according to claim 138, wherein at least other one dielectric

sub-layer is formed over the passivation layer and covers the formed conductive metal after the sequential steps 7-12 are repeated at least one time.

140. The process according to claim 139, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

141. The process according to claim 139, wherein the other dielectric sub-layer is made of an organic compound.

142. The process according to claim 139, wherein the other dielectric sub-layer is made of a macromolecule polymer.

143. The process according to claim 139, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

144. The process according to claim 122, wherein the thickness of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 50 microns.

145. The process according to claim 122, wherein the width of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 1 centimeter.

146. The process according to claim 122, wherein the cross-sectional area of the trace constructed of the conductive layer and the conductive metal ranges from 1 square micron to 0.5 square millimeters.

147. The process according to claim 122, wherein the passivation layer is

constructed of an inorganic compound.

148. The process according to claim 122, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

149. The process according to claim 122, wherein, before the step 2 is performed, a dielectric sub-layer is formed on the passivation layer, the dielectric sub-layer includes at least one via metal opening connecting with the opening of the passivation layer, and, then, when the step 2 is performed, the conductive layer is formed on the dielectric sub-layer, the side wall of the via metal opening, and the interconnection scheme exposed by the opening of the passivation layer.

150. The process according to claim 149, wherein the largest width of the via metal opening is larger than that of the opening of the passivation.

151. The process according to claim 149, wherein the cross-sectional area of the via metal opening ranges from 1 square micron to 10,000 square microns.

152. The process according to claim 149, wherein the largest width of the opening of the passivation ranges from 0.5 microns to 200 microns.

153. The process according to claim 122, wherein during the step 2, a sputtering process is used to form the conductive layer over the passivation layer of the wafer.

154. The process according to claim 122, wherein during the step 4, an electroplating process is used to fill the conductive metal over the conductive layer.

155. The process according to claim 122, wherein the material of the

conductive layer includes titanium-tungsten alloy, titanium or chromium.

156. The process according to claim 122, wherein the material of the conductive metal includes copper, nickel, or gold.

157. The process for fabricating a chip structure, comprising:

Step 1: providing a wafer with a plurality of electric devices, an interconnection scheme and a passivation layer, the electric devices and the interconnection scheme arranged inside the wafer, the interconnection scheme electrically connected with the electric devices, the passivation layer disposed on a surface layer of the wafer, the passivation layer having at least one opening exposing the interconnection scheme, wherein the largest width of the opening of the passivation ranges from 0.5 microns to 20 microns;

Step 2: forming a conductive layer over the passivation layer of the wafer, and the conductive layer electrically connected with the interconnection scheme;

Step 3: forming a photoresist onto the conductive layer, and the photoresist having at least one opening exposing the conductive layer;

Step 4: filling at least one conductive metal into the opening of the photoresist, and the conductive metal disposed over the conductive layer;

Step 5: removing the photoresist; and

Step 6: removing the conductive layer not covered with the conductive metal.

158. The process according to claim 157, wherein a dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after step 6 is performed.

159. The process according to claim 158, wherein at least one node opening is formed through the dielectric sub-layer to expose the conductive metal formed at a lower portion after the dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

160. The process according to claim 158, wherein the dielectric sub-layer is made of an organic compound.

161. The process according to claim 158, wherein the dielectric sub-layer is made of a macromolecule polymer.

162. The process according to claim 158, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

163. The process according to claim 157, wherein the process further comprises:

Step 7: forming a dielectric sub-layer over the passivation layer, the dielectric sub-layer covering the formed conductive metal, and the dielectric sub-layer having at least one opening exposing the conductive metal formed at a lower portion;

Step 8: forming at least other one conductive layer on the dielectric sub-layer and into the opening of the dielectric sub-layer, and the other conductive layer electrically connected with the metal layer exposed by the opening of the dielectric sub-layer;

Step 9: forming a photoresist onto the other conductive layer, and the photoresist having at least one opening exposing the other conductive layer;

Step 10: filling at least other one conductive metal into the opening of the

photoresist, and the other conductive metal disposed over the other conductive layer;

Step 11: removing the photoresist; and

Step 12: removing the other conductive layer not covered with the other conductive metal.

164. The process according to claim 163, wherein the dielectric sub-layer is made of an organic compound.

165. The process according to claim 163, wherein the dielectric sub-layer is made of a macromolecule polymer.

166. The process according to claim 163, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

167. The process according to claim 163, wherein the thickness of the dielectric sub-layer ranges from 1 micron to 100 microns.

168. The process according to claim 163, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the step 12 is performed.

169. The process according to claim 168, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

170. The process according to claim 168, wherein the other dielectric sub-layer is made of an organic compound.

171. The process according to claim 168, wherein the other dielectric sub-

layer is made of a macromolecule polymer.

172. The process according to claim 168, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

173. The process according to claim 163, wherein the sequential steps 7-12 are repeated at least one time.

174. The process according to claim 173, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the sequential steps 7-12 are repeated at least one time.

175. The process according to claim 174, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

176. The process according to claim 174, wherein the other dielectric sub-layer is made of an organic compound.

177. The process according to claim 174, wherein the other dielectric sub-layer is made of a macromolecule polymer.

178. The process according to claim 174, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

179. The process according to claim 157, wherein the thickness of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 50 microns.

180. The process according to claim 157, wherein the width of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 1 centimeter.

181. The process according to claim 157, wherein the cross-sectional area of the trace constructed of the conductive layer and the conductive metal ranges from 1 square micron to 0.5 square millimeters.

182. The process according to claim 157, wherein the passivation layer is constructed of an inorganic compound.

183. The process according to claim 157, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

184. The process according to claim 157, wherein, before the step 2 is performed, a dielectric sub-layer is formed on the passivation layer, the dielectric sub-layer includes at least one via metal opening connecting with the opening of the passivation layer, and, then, when the step 2 is performed, the conductive layer is formed on the dielectric sub-layer, the side wall of the via metal opening, and the interconnection scheme exposed by the opening of the passivation layer.

185. The process according to claim 184, wherein the largest width of the via metal opening is larger than that of the opening of the passivation.

186. The process according to claim 184, wherein the cross-sectional area of the via metal opening ranges from 1 square micron to 10,000 square microns.

187. The process according to claim 157, wherein during the step 2, a

sputtering process is used to form the conductive layer over the passivation layer of the wafer.

188. The process according to claim 157, wherein during the step 4, an electroplating process is used to fill the conductive metal over the conductive layer.

189. The process according to claim 157, wherein the material of the conductive layer includes titanium-tungsten alloy, titanium or chromium.

190. The process according to claim 157, wherein the material of the conductive metal includes copper, nickel, or gold.

191. The process for fabricating a chip structure, comprising:

Step 1: providing a wafer with a plurality of electric devices, an interconnection scheme and a passivation layer, both the electric devices and the interconnection scheme arranged inside the wafer, the interconnection scheme electrically connected with the electric devices, the passivation layer disposed on a surface layer of the wafer, the passivation layer having at least one opening exposing the interconnection scheme;

Step 2: forming at least one conductive metal over the passivation layer of the wafer, and the conductive metal electrically connected with the interconnection scheme;

Step 3: forming a photoresist onto the conductive metal, and patterning the photoresist to expose the conductive metal to the outside;

Step 4: removing the conductive metal not covered with the photoresist; and

Step 5: removing the photoresist.

192. The process according to claim 191, wherein a dielectric sub-layer is

formed over the passivation layer and covers the formed conductive metal after step 5 is performed.

193. The process according to claim 192, wherein at least one node opening is formed through the dielectric sub-layer to expose the conductive metal formed at a lower portion after the dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

194. The process according to claim 192, wherein the dielectric sub-layer is made of an organic compound.

195. The process according to claim 192, wherein the dielectric sub-layer is made of a macromolecule polymer.

196. The process according to claim 192, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

197. The process according to claim 191, wherein a conductive layer, the material of which includes titanium-tungsten alloy, titanium or chromium, is formed over the passivation layer of the wafer before the step 2 is performed, and then the conductive metal is formed on the conductive layer when the step 2 is performed.

198. The process according to claim 197, wherein a sputtering process is used to form the conductive layer over the passivation layer of the wafer.

199. The process according to claim 197, wherein an electroplating process or a sputtering process is used to form the conductive metal on the conductive layer.

200. The process according to claim 191, wherein the process further comprises:

Step 6: forming a dielectric sub-layer over the passivation layer, the dielectric sub-layer covering the formed conductive metal, and the dielectric sub-layer having at least one opening exposing the conductive metal formed at a lower portion;

Step 7: forming at least other one conductive metal over the passivation layer of the wafer, and the other conductive metal electrically connected with the conductive metal formed at a lower portion;

Step 8: forming a photoresist onto the other conductive metal, and patterning the photoresist to expose the other conductive metal to the outside;

Step 9: removing the other conductive metal not covered with the photoresist; and

Step 10: removing the photoresist.

201. The process according to claim 200, wherein the dielectric sub-layer is made of an organic compound.

202. The process according to claim 200, wherein the dielectric sub-layer is made of a macromolecule polymer.

203. The process according to claim 200, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

204. The process according to claim 200, wherein the thickness of the dielectric sub-layer ranges from 1 micron to 100 microns.

205. The process according to claim 200, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the step 10 is performed.

206. The process according to claim 205, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

207. The process according to claim 205, wherein the other dielectric sub-layer is made of an organic compound.

208. The process according to claim 205, wherein the other dielectric sub-layer is made of a macromolecule polymer.

209. The process according to claim 205, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

210. The process according to claim 205, wherein a conductive layer is formed onto the dielectric sub-layer before the step 7 is performed, and, then, the conductive metal is formed on the conductive layer when the step 7 is performed.

211. The process according to claim 200, wherein the sequential steps 6-10 are repeated at least one time.

212. The process according to claim 211, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the sequential steps 6-10 are repeated at least one time.

213. The process according to claim 212, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

214. The process according to claim 212, wherein the other dielectric sub-layer is made of an organic compound.

215. The process according to claim 212, wherein the other dielectric sub-layer is made of a macromolecule polymer.

216. The process according to claim 212, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

217. The process according to claim 191, wherein the thickness of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 50 microns.

218. The process according to claim 191, wherein, before the step 2 is performed, a dielectric sub-layer is formed on the passivation layer, the dielectric sub-layer includes at least one via metal opening connecting with the opening of the passivation layer, and, then, when the step 2 is performed, the conductive metal is formed on the dielectric sub-layer and into the via metal opening.

219. The process according to claim 218, wherein the largest width of the via metal opening is larger than that of the opening of the passivation.

220. The process according to claim 191, wherein the material of the conductive metal includes aluminum, copper, nickel, or gold.